AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): A scanning circuit comprising:

a bidirectional shift register having transfer gates of a transfer unit and a feedback circuit, the operation of which is controlled by four phase clocks,

wherein said scanning circuit comprises a delay circuit that delays control clocks supplied to said transfer gates of the transfer unit relative to control clocks supplied to said feedback circuit.

2. (currently amended): A scanning circuit comprising:

a transfer unit comprising a plurality of stages of transfer gates which are in series connected to each other;

a plurality of feedback circuits which are connected to connecting points between said transfer gates,

said feedback circuits eliminating amplitude attenuation of signals transferred through said transfer unit,

wherein said scanning circuit comprises a delay circuit that delays control clocks controlling operation timing of the transfer gates of the transfer unit relative to control clocks controlling operation timing of said feedback circuit.

3. (currently amended): A scanning circuit comprising:

a transfer unit comprising a plurality of stages of transfer gates which are in series connected with each other, and a plurality of feedback circuits which are connected to connecting points between said transfer gates,

said feedback circuits eliminating amplitude attenuation of signals transferred via said transfer unit,

(a) wherein said scanning circuit comprises:

a phase control circuit having an input terminal receiving two-phase clocks and outputting a signal obtained by non-inverting/inverting said received two-phase clocks based upon a value of a control signal, and a

delay circuit,

(b) wherein ~~the~~ two-phase clocks from said delay circuit are delayed relative to the two-phase clocks output from the phase control circuit, and

(c) wherein the two-phase clocks which have been delayed by said delay circuit are supplied to the transfer gates of the transfer unit, and the two-phase clocks from said phase control circuit are supplied to said feedback circuits.

4. (original): The scanning circuit as defined in Claim 2 wherein each of said feedback circuits comprises:

a first inverter having an input terminal connected to a connection point between transfer gates which form the transfer unit, and

a second inverter having an input terminal connected to an output terminal of said first inverter and an output terminal connected to the input terminal of said first inverter via a transfer gate which is turned on or off in response to the clocks supplied to the feedback circuit.

5. (original): The scanning circuit as defined in Claim 3 wherein each of said feedback circuits comprises:

a first inverter having an input terminal connected to a connection point between transfer gates which form the transfer unit, and

a second inverter having an input terminal connected to an output terminal of said first inverter and an output terminal connected to the input terminal of said first inverter via a transfer gate which is turned on or off in response to the clocks supplied to the feedback circuit.

6. (original): The scanning circuit as defined in Claim 2 wherein each of said feedback circuits comprises:

a first inverter having an input terminal connected to a connection point between transfer gates which form the transfer unit, and

a clocked inverter having an input terminal connected to an output terminal of said first inverter and an output terminal connected to the input terminal of said first inverter, said clocked inverter being turned on or off in response to the clocks supplied to the feedback circuits.

7. (original): The scanning circuit as defined in Claim 3 wherein each of said feedback circuits comprises:

a first inverter having an input terminal connected to a connection point between transfer gates which form the transfer unit, and

a clocked inverter having an input terminal connected to an output terminal of said first inverter and an output terminal connected to the input terminal of said first inverter, said clocked inverter being turned on or off in response to the clocks supplied to the feedback circuits.

8. (original): A scanning circuit, wherein said scanning circuit comprises:

(a) a transfer unit having a plurality of stages of transfer gates which are in series connected to each other, said transfer gates delaying and transferring input pulse signals;

(b) a plurality of feedback circuits including two stage inverters, each of said feedback circuits being connected to a connecting point between said transfer gates and have input and output terminals which are connected to each other via a switch; and

(c) a delay circuit that delays a phase of a clock controlling timing relationship of turning on or off of the transfer gates of said transfer unit relative to the phase of the clock controlling timing relationship of turning on or off of said feedback circuits.

9. (currently amended): A scanning circuit comprising:

(a) a transfer unit having a plurality of stages of transfer gates which are in series connected to each other to delay and transfer input pulse signals;

(b) a plurality of feedback circuits each including an inverter and a clocked inverter, each of said feedback circuits being connected to a connecting point between said transfer gates and having input and output terminals which are connected to each other for feedback; and

(c) a delay circuit that delays a phase of a clock for controlling timing relationship of turning on or off of the transfer gates of said transfer unit relative to a phase of a clock for controlling timing relationship of turning on or off of the clocked inverter of said feedback circuit.

10. (original): The scanning circuit as defined in Claim 8, wherein said scanning circuit further comprises a phase control circuit having an input terminal to which two-phase clocks are input to output signals obtained by non-inverting/inverting said input two-phase clocks based upon a value of a control signal for controlling a shift direction, and

wherein said delay circuit delays input two-phase clocks relative to said signals of two-phase clocks output from said phase control circuit.

11. (original): The scanning circuit as defined in Claim 9, wherein said scanning circuit further comprises a phase control circuit having an input terminal to which two-phase clocks are

input to output signals obtained by non-inverting/inverting said input two-phase clocks based upon a value of a control signal for controlling a shift direction, and

wherein said delay circuit delays saidinput two-phase clocks relative to said signals of two-phase clocks output from said phase control circuit.

12. (original): The scanning circuit as defined in Claim 1, wherein said scanning transfer unit comprises an input terminal which receives an input signal, said input terminal being connected to one end and the other end of said bidirectional shift register.

13. (original): The scanning circuit as defined in Claim 2, wherein said scanning transfer unit comprises an input terminal which receives an input signal, said input terminal being connected to one end and the other end of said transfer unit.

14. (original): The scanning circuit as defined in Claim 3, wherein said scanning transfer unit comprises an input terminal which receives an input signal, said input terminal being connected to one end and the other end of said transfer unit.

15. (original): The scanning circuit as defined in Claim 8, wherein said scanning transfer unit comprises an input terminal which receives an input signal, said input terminal being connected to one end and the other end of said transfer unit.

16. (original): The scanning circuit as defined in Claim 9, wherein said scanning transfer unit comprises an input terminal which receives an input signal, said input terminal being connected to one end and the other end of said transfer unit.